Printed Flexible Organic Transistors with Tunable Aspect Ratios

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A fabrication technique that allows aspect ratio modulation in a large array of organic thin film transistors (OTFTs) is demonstrated. In this design, discrete interdigitated source and drain electrodes can be individually selected to create a range of aspect ratios (W/L). It is shown that by increasing the aspect ratio, the drain current is increased respectively. Arrays of OTFTs are fabricated with a combination of inkjet printing and surface energy patterned blade coating. OTFTs with optimized aspect ratios are interconnected to form electronic circuits with the desired performance. A fabricated enhancement-load inverter with selected aspect ratios of 2000 μm/50 μm for the drive OTFT and 250 μm/50 μm for the load transistor show good switching performance with a dc gain of approximately 6 at supply voltage of −20 V.

1. Introduction

Over the past several years, many large-area printed electronics have demonstrated significant benefit from their utilization of organic thin-film transistors (OTFTs), where inexpensive and fast fabrication techniques using solution-processing materials have shown great promise.[1–3] Crystalline silicon technology can be challenging to apply in fabrication and distribution of electronics over a large area, mainly due to high processing and manufacturing cost per unit area in addition to the high cost of single crystal wafer substrates. Low temperature simplified solution-processing techniques minimizes materials waste and has the potential to replace some expensive procedures. This has made OTFT technology an increasing constituent of large-area electronics, both at device and integrated circuits level.[4–8] Solution-processed small-molecule organic semiconductors (SOCs) are successfully used as active layers of OTFTs, which find applications in active-matrix electronic-paper displays, organic light-emitting diode displays, circuits for radiofrequency identification RFID, and simple logic circuits.[9–12] The recent advancements of solution-processed SOCs used in thin film transistor show device performance reaching that of amorphous Si and solution-processed metal oxides. This high performance makes SOCs p-type OTFTs a strong candidate for several future complementary metal-oxide semiconductor applications.[13–15] Modulation of scale ratio of devices in a large array is one of the important parameters that governs circuit design. While most printing techniques can provide faster fabrication processes, the rapid on-demand modulation of W/L scale ratio in large array of devices remains as a challenge and a topic to investigate; especially for the myriad of specified circuit designs and application requirements. For instance, the tuning of the gain in each stage of an amplifier[16–18] or logic circuits[5] requires the modulation of OTFT W/L ratio. These configuration changes can be challenging, costly, and time consuming for common electrode printing techniques, such as screen printing and gravure printing.[19–22] These conventional mask-based approaches utilize a fixed pattern transfer that requires a full re-design for every new device structure.[21,23,24] Inkjet printing on the other hand is a nonimpact digital prototyping method that provides instant change of patterns.[25,26] This elimination of mask can reduce the processing costs especially for large-scale production.[27] However, throughput of inkjet printing can become a limiting factor, especially when depositing over large area.[28] Interdigitated source and drain structure have been used in previous reports as a method to modify W/L ratio for a specific circuit design.[17,29–31] The channel width (W) is modulated by changing the finger count. Meanwhile, channel length (L) is the smallest space between source and drain electrodes, and the resolution is associated to the printing technique. Low switching speed is one of the drawbacks of printed OTFTs compared to conventional Si technology, which can result from a number of factors such as mobility, dielectric layer thickness, and channel length. Achieving channel lengths smaller than 10 μm while maintaining high device yield is very challenging with printing techniques, especially for low-viscosity inks. The solution found to overcome this challenge is to utilize a combination of patterning techniques including the combination of conventional photolithography and direct-write printing techniques.[32] In parallel, there has been an interest to develop methods to decrease the source and drain electrode geometry and channel length using many printing methods. Interdigitated source and drain (SD) electrodes are typically used in electronics to increase channel width while maintaining small channel lengths, resulting in higher W/L ratios. There are few reports on printed interdigitated...
electrodes, and all of them are achieved with a combination of photolithographic and printing methods. In this work, the electrode geometry is optimized for surface energy patterned (SEP) blade coating in order to achieve 50 µm channel length using interdigitated SD geometry with 100% yield using low-viscosity PEDOT:PSS solution. In addition, the method describes how different pairs of electrodes can be selected by printing in order to modulate, on demand, the \( W/L \) ratios of a large array of devices. This method uses only direct-write printing techniques and results in high yields and a range of \( W/L \) ratio values which is needed for device integration into circuits.

## 2. Results

OTFT arrays are fabricated using a combination of surface energy patterning, blade coating, and inkjet printing. A hydrophobic self-assembled monolayer (SAM), fluroalkylsilane, is deposited on the plastic substrate and patterned by etching the monolayer through a stainless-steel mask with low energy plasma. The steps of this process are shown in Figure S1, Supporting Information. The complete process flow used for fabrication of discrete devices is given in Figure 1a. The stainless-steel mask defines hydrophilic regions which will form the SD electrodes. We use blade coating to deposit PEDOT:PSS as a conducting material for SD electrodes. Eleven interdigitated electrodes are printed in an area of 1700 × 980 µm\(^2\) with a separation of 50 µm, shown in Figure 1b. The gap between electrodes defines the channel length of a given OTFT in the array. Subsequently inkjet printing is utilized to print Ag nanoparticles onto contact pads of each electrode. It is at this stage in the fabrication that a given width transistor can be defined. Printing Ag contacts on all of eleven electrodes would result into channel width \( W \) of 2500 µm with the channel length \( L \) set by the 50 µm distance between electrodes. Blade coating is used to deposit semiconductor and the gate dielectric layer over the entire area, covering all of the eleven electrodes. The optical microscopy of the channel along with the previous steps is shown in Figure 1c. While the gate dielectric, 120 nm thick, fully covers the channel it leaves the ink jetted Ag contacts exposed. These contacts are typically 300 nm thick and are protruding over the dielectric layer. At the final stage of device fabrication, the gate electrode is deposited by thermal evaporation together with parallel metal bars that connect the selected SD electrodes (electrodes with printed Ag contact pads). The top view schematic and cross-section of the interdigitated device structure are shown in Figure 1e,f. The optical micrograph of a portion of an array of printed OTFTs with different \( W/L \) ratios is shown in Figure 2d.

*Figure 1. a) The printing and fabrication steps for OTFTs using self-assembled energy patterning blade coating for discrete source-drains and semiconductor channels, inkjet printing contacts, blanket coating a dielectric layer, and gate and finger-connection evaporation. b) Optical microscopy image of blade coated PEDOT:PSS interdigitated sources and drains electrodes. c) Blade coated dif-TES-ADT:PTAA semiconductor film and the inkjet-printed contacts on the electrodes. d) Optical microscopy images of two OTFTs and zoomed-out digital image of a portion of array of devices with various \( W/L \) ratios. e) Top-view schematic of the device structure. f) Cross-section view of the device.*
The number of on-demand inkjet-printed source and drain contacts can digitally modulate drain current ($I_D$) as follows:

$$I_D \propto (n-1) \times \frac{W}{L}; 1 \leq n \leq 10$$

(1)

where $n$ is the number of inkjet-printed contacts on discrete source and drain electrodes. By increasing $n$, $W$ is increased while $L$ is kept constant. The increase of $W$ increases $I_D$. For example, a device with $n = 5$ has the $W/L$ of (1000 µm/50 µm). The transfer characteristics of three typical devices with $n = 3$, 8, 11 are shown in Figure 2a–c. The output characteristics of these devices are shown in Figure 2d–f. The gate leakage currents associated with those three devices are demonstrated in Figure 2g–i.

By adding to the number of active channels, $I_D$ is increasing as expected. The variability in change of $I_D$ is later studied and explained by crystal structure of the semiconductor channel.

The performance of the device indicates no contact barrier, high output resistance, good square law, and low $I_{OFF}$ current.

Performance of OTFTs is characterized by studying 64 single channels. A single channel, shown in Figure 3a, is defined as the active channel area between two contact-printed discrete source and drain electrodes. The selected single channels are along an array where their DC electrical characteristics are measured and characterized in air by output characteristic curves derived for each channel.

The $V_T$ is found by the interception of the fitting curve to the $(V_D-V_G)$ plot as shown in Figure 3b. The saturation mobility was calculated from transfer characteristics $I_D-V_G$ in the saturation regime plotted as $V_G$–$V_G$ and the $\mu$ is calculated using the $I_D$ saturation equation as follows:

$$\mu = \frac{2L}{WC} \left( \frac{dV_D}{dV_G} \right)^2$$

(2)
Figure 3c demonstrates an example of subthreshold slope (SS) derivation, which is defined to be the inverse slope of the log \( I_D \) versus \( V_{GS} \) in the subthreshold region. The SS, \( V_T \), \( \log(I_{ON}/I_{OFF}) \), and \( \mu \) statistical distributions of 64 single channels are shown in Figure 3d. The mean subthreshold swing is 1.39 V/dec. For these channels, the average threshold voltage is \(-0.96 \) V with a 1.07 standard deviation and the mean mobility of the devices is \(0.38 \) cm\(^2\) V\(^{-1}\) s\(^{-1}\) with a standard deviation of 0.23.

The electrical characteristics of individual device channels are demonstrated in Figure S2a, Supporting Information, showing variations in \( V_{th} \), \( \mu \), and SS for adjacent channels in a single device. In order to study underlying reasons for such variations, atomic force microscopy (AFM) was utilized to obtain information on the morphology and surface features of the individual channels. AFM images of random spots along individual channels in a typical device are shown in Figure S2b, Supporting Information. The images are readily interpretable as presence of a number of crystalline domains with different orientations (along the source electrode to drain) and well-defined boundaries that extend up to tens of microns which is largely in agreement with the literature.\(^{[35–37]}\)

Importance of good connectivity between domains and well-aligned crystallography across transistor channels has been previously highlighted as these features have been shown to greatly influence charge mobility and performance as well as device-to-device variability due to presence of deep charge traps in the boundaries.\(^{[35,36,38–42]}\) Moreover, domains show distinctive ribbed thickness variations and needle-like crystallites are occasionally apparent at the boundaries. These have been previously correlated with poorer device performance due to hindrance in charge transport across domains in the channels.\(^{[41–45]}\)

Digital circuit functionality can be maintained in different ways including static and dynamic logic. The reliability of this fabrication technique was proven through the demonstration of static logic inverters, which are the most fundamental element of a more complicated digital circuit. Figure 4a shows the circuit schematic of an enhancement-load inverter with two OTFTs, one operating as the drive transistor and the other as the load transistor. The drive transistor turns ON with the supply voltage \( V_{DD} \) applied to the gate of the drive transistor \( V_{in} \) (input node). Then the resistance becomes significantly smaller than the load transistor and the output voltage is pulled to the ground voltage considered as logic “0”. With logic “0” applied to the input voltage, the drive transistor is OFF and the saturated-load transistor pulls the voltage at the output node to a difference value between the supply voltage \( V_{DD} \) and the threshold voltage, which is logic “1”. Figure 4b shows and compares the electrical transfer characteristics of two inverters. The voltage gain, the maximum small signal amplification, of the enhancement-load inverter is determined by the ratio of scale factor of the two devices:

\[
\frac{dV_{out}}{dV_{in}} = \frac{W_{drive} \times L_{load}}{W_{load} \times L_{drive}}
\]  

This equation is derived under the assumption that the load and drive transistors both have the same electrical characteristic of \( V_{th} \) and \( \mu \). For OTFTs with variabilities in electrical characteristics, the equation is legitimate, and the gain is proportional to the ratio of the scale factors. Of the two inverters, in Figure 4b, one has \( W_{Drive} \) of 2000 \(\mu\)m and the other with \( W_{Drive} \) of 1000 \(\mu\)m, both with the same channel length of 50 \(\mu\)m. The inverters show satisfactory transfer characteristics as expected.
The increase of $W_{\text{Drive}}$ results in higher voltage gain and improvement in the noise margin. Figures 4c and 4d show obtained voltage transfer curves and signal voltage gain with $V_D$ supply voltages of $-4$ to $-20$ V.

### 3. Conclusion

In conclusion, we have demonstrated a fast fabrication method for on-demand modulation of scale ratio along a large array of devices. The combination of inkjet printing for channel modulation with SEP blade coating is proper for large area electronics due to fast fabrication and change of channel width without the need for change of the process for a new design. Devices exhibit an expected change in output characteristics with modulation of channel width from 250 to 2500 µm. The individual channels show good average subthreshold swing of 1.39 V/dec, threshold voltage of $-0.96$ V with a standard deviation of 1.07 and mobility of the devices is 0.38 cm² V⁻¹ s⁻¹. The variability witnessed in the electrical characteristics of devices is inherent in the nature of variation in the printing techniques and most importantly resulted from the lack of control in the formation of the crystal structure. Despite the variations, we have been able to fabricate enhancement-load inverters with good voltage transfer curves. An inverter with selected $W_{\text{Drive}}$ of 2000 µm has a dc gain of 6 with supply voltage of $-20$ V.

### 4. Experimental Section

**Blade Coater and Inkjet Setup:** A doctor blade (Zehntner ZUA 2000.60 Universal Applicator) with adjustable gap height was used to coat conductor and semiconductor layers to form SD electrodes and channel accordingly. A four-sided cylindrical doctor blade (ZFR 2040.6030) was used to coat a gate dielectric layer. Two controllable-speed blade coating setup with a linear servo (Servo City) were used to actuate the blades. An inkjet printer (Dimatix DMP-2831) was used to print the discrete finger contact pads. Stainless-steel masks were fabricated by Photo Etch Technology. Oxygen plasma system (Diener Nano) was used for the SEP processes. An air plasma (PLASMOD) was used for cleaning substrates.

**Array Fabrication:** Top-gate array of DI-OTFTs was fabricated on a laser-cut 90 × 105 mm polyethylene naphthalate (PEN) (Dupont PQA1) substrate. The sample was rinsed in isopropanol, dried with a nitrogen gun, and then plasma cleaned for 10 s followed by a 20 min surface
treatment step in which a monolayer of (heptadecafluoro-1,1,2,2-tetraphenylhexyl) and trichlorosilane (FDTS, Celest SH5841.0) was deposited on the sample for 20 min under light vacuum (0.1–1 torr). The SEP step was done by pressing the stainless-steel mask, with the source and drain patterns and rectangular reservoir, on top of the substrate. After dispensing 35 µL of PEDOT:PSS (Sigma-Aldrich 739316-25G) diluted by 10 min. 90 s of semiconductor (10 mg mL−1) of (250 W/L µm) was used for the second SEP under the same conditions except this time, with a timing of 0.7 min. The sample was soaked and cleaned in toluene for 10 min. The source and drain contact pads were inkjet-printed with silver nanoparticles (Suntronic JetSilver EMDS30) and then annealed at 120 °C for 10 min. Another FDTS surface treatment was done after removing the previous monolayer by a 10 s plasma cleaning. A plasma cleaning was done for 10 s to remove the first monolayer before the second FDTS surface treatment. Another mask that had the rectangular-shaped channel patterns with (W/L) of (250 µm/50 µm) was used for the second SEP under the same conditions except this time, with a timing of 0.7 min. The sample was soaked and cleaned in toluene for 30 s. The semiconductor was the mix of small molecule 2,8-difluoro-5,11-bis(3-triethylsilylphenyl)anthradithiophene (dif TES ADT) and the low mobility amorphous polymer poly[bis(4-phenyl)(2,4,6-trimethylphenyl)amine] (PTAA). 13 µL of semiconductor (10 mg mL−1 of 1:1 dif TES ADT:PTAA in 2:1 mesitylene:etetrailin) in small drops was added in front of the blade on either the left or the right side of the sample, the drops were then uniformly spread as the blade was dragged. The blade coating was done in the glove box on a 35 °C hot plate at 200 µm height and 1–2 cm s−1 speed. The annealing was done by ramping the temperature up from 35 to 120 °C for 10 min and then turning off the plate to cool down for 10 min. 90 µL of amorphous fluoropolymer (DuPont AF) was diluted by 20 vol % in FC770 fluororesolvent and then blade coated on a vacuum plate across the whole sample at a blade height of 50 µm and speed of 2 cm s−1 from top to bottom. After blade coating, the substrate stayed on the vacuum plate for an hour and then annealed at 120 °C for 10 min. The final step was the evaporation of the gate and the contact pad connection lines using a stainless-steel mask. 65 nm aluminum was evaporated at a base pressure of 2 × 10−5 torr.

**AFM Imaging:** AFM topology images were obtained using an MFP-3D Origin+AFM (Asylum Research, Santa Barbara, USA) Instrument operated in AC tapping mode in air utilizing a PointProbe-Plus cantilever (PPP-NCHR, Nanosensors, Neuchâtel, Switzerland) with a nominal radius of less than 10 nm. Images were collected at 1024 × 1024 resolution with a scan rate of 0.8 Hz and were processed using the Gwyddion image-processing software.

**Supporting Information**

Supporting Information is available from the Wiley Online Library or from the author.

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**Conflict of Interest**

The authors declare no conflict of interest.

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